Design and Implementation of Two Input Modified Single Ended Primary Inductance Converter for Micro Grid Application

Hemalatha J N
Department of Electrical & Electronics Engineering, RV College of Engineering, Bengaluru, India.

Hariprasad S A
Department of Electronics & Communication Engineering, Jain School of Engineering, Bengaluru, India.

Anitha G S
Department of Electrical & Electronics Engineering, RV College of Engineering, Bengaluru, India.

Abstract – The critical component of a hybrid renewable resources based system is the power electronic interface connected between source and load. The primary goal of this interface is to maintain constant output voltage with high efficiency at all operating points, irrespective of variations in the input levels. In conventional distributed generation system employing multiple renewable resources requires separate power electronic converter for every source to maintain constant output voltage as the input is highly fluctuating. Also every converter stage requires its own controller to balance the power. Generally the devices used in power converters operates in hard switching mode of devices, this not only increases the switching loss but also the switching stress across the device at every switching cycle. Therefore the operating life time of the system reduces. The primary objective of this paper is to design and implement a dual input modified Single Ended Primary Inductance Converter to meet the requirements of reduced stress, high efficiency and constant output voltage at different conditions when compared to conventional SEPIC topology. In this paper an attempt is made to propose a modified converter topology by providing lossless passive snubber for each switching device in each stage focusing on the reduction of large dv/dt and large di/dt to reduce the switching stress across the switching device and also to improve the efficiency by achieving zero current switching at turn on and zero voltage switching at turn off. The proposed topology is validated in MATLAB Simulink platform considering solar PV model and wind model as its inputs individually and simultaneously. Also it is been validated with a master controller to regulate the output voltage by controlling the duty cycle of the switches. The results were analysed to show that the switching stress is less and efficiency is high at different operating conditions. The power simulation results shows that the stress across the device is reduced by 4% and efficiency improved by 4% as compared to conventional SEPIC topology. The dual input converter is practically implemented and tested.

Index Terms – Distributed generation, switching stress, Multi Input Converter, micro-grid, passive lossless snubber.

1. INTRODUCTION

Renewable resources are the promising energy sources for power generation across the globe due to rapid depletion of fossil fuels used for electric energy production, increased global warming, and pollution. As the availability of the resources is dependent on the weather conditions, the challenging task is to maintain continuity of power supply. An easy solution to provide uninterrupted power supply is to combine different sources that are complement to each other. Power electronic converter plays a vital role in power generation using renewable sources. Diverse renewable energy sources are connected to a common load through a number of single-input single output converters. Multiple sources needs individual converters that requires separate controllers to maintain constant DC voltage at the bus. This disadvantage is overcome by using Multiple Input Converter (MIC) configuration. MIC uses a single controller to maintain the power balance [1]-[5]. MIC topology reduces the complexity with less components and hence improve system reliability with less cost. The conventional Single Ended Primary Inductance Converter involves in hard switching of the devices. So the voltage stress across the switching device is too large that makes the reliability and efficiency of the system at stake in whatever the domain the converter used. Many researchers in past, proposed different techniques for the synthesis of multiple input converters in literature. [6]- [8] describes the detailed procedure to derive multi input converters by following certain rules for the existing basic converters. Multi input converter proposed for micro grid application in literature employs individual separate converters for every source using independent controller, so the flexibility in control and reliability is the major limitation[9]-[10]. Few multi input converters proposed [11] describes about dual input cuk-SEPIC topology, the operational efficiency is less and

voltage stress across the device is more as hard switching is used. The limitation of lesser efficiency was overcome with SEPIC-SEPIC, but even this topology suffer with high voltage stress across the device. Soft switching techniques are most suitable for reducing the stress. The large dv/dt and large di/dt across the device are reduced by utilizing snubber elements and circuits. Passive snubber circuit though reduces the stress but adds on to power loss because of passive elements, active snubber circuit requires another switching device. In the literature many papers on passive lossless snubber circuit were proposed.

Describe complete analysis of, how to place the snubber elements in the circuit to have less stress across the device with improved efficiency and recovering the energy stored in inductive elements. Conventional SEPIC topology utilise hard switching concept where the device undergoes a severe voltage and current stress during each switching operation. The passive lossless snubber circuit along with the switching device soft switching can be achieved. This part of the circuit is significant only during short interval of time which gives ZCS switching operation and the energy is recovered instead of wasting the energy in normal RCD snubber circuit. Also the non idealities of the circuit such as on state resistance of the devices, internal resistance for the significant passive components in the circuit are also considered for the performance analysis of the converter.

Fig 1 shows the circuit schematic of passive lossless snubber for conventional SEPIC topology that works with ZCS during turn on and ZVS during turn off, so the voltage and current stress across the device is lesser. The analysis is divided into eight modes of operation, the detailed analysis, design and simulation is presented in [12]. The snubber circuit is effective during the transient period where as in the rest of the switching period the converter behaves in the same way as normal PWM converter. The normal SEPIC topology (without snubber) and modified SEPIC are simulated in MATLAB the. The results are tabulated in table 1. As an extension to the proposed topology is tested for dual input configuration. This paper focusses on the performance analysis of dual input modified SEPIC.

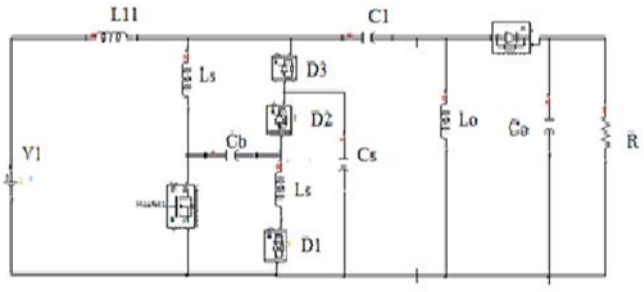


Fig 1: modified SEPIC circuit

Table 1. Performance parameters of the proposed converter and conventional converter

Topology	Input current ripple in A	Output current ripple A	Output voltage ripple in A	Switch stress in W	Input Power	Output Power	Efficiency
Proposed	0.71-0.689=0.021	3.185-3.144=0.041	6.37-6.28=0.09	125	23.07	20.7	89.6
Conventional	2.47-2.44=0.03	6-5.85=0.15	12-11.82=0.18	165	77	66	85

Fig 2 depicts the block diagram of the proposed work. Integration of two converters into one converter has many benefits like reduced component count, less ripple and better efficiency compared to normal two input SEPIC. This paper proposes analysis of dual input modified SEPIC topology in steady state operation.

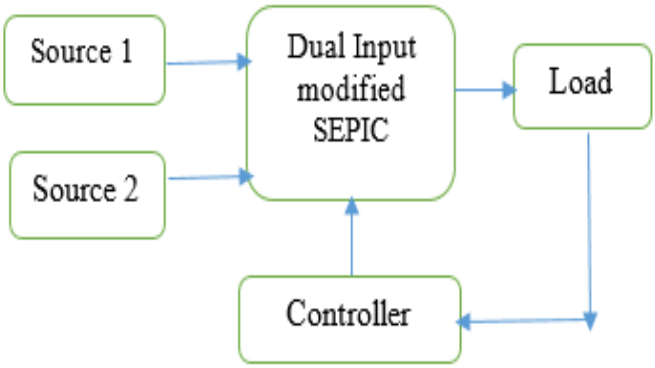


Fig 2. Block diagram of the proposed topology

Two different renewable energy sources such as solar and wind energy resources are fed to the load through the modified converter. In order to maintain output voltage constant, the duty ratios of 2 switches of the converters are varied and are controlled by PID controller. The proposed converter will be able to transfer energy to the load individually or simultaneously. The proposed dual input converter is developed to maintain output voltage constant with variations of input sources and load.

The paper is organized in following sections section II gives brief analysis and design of the circuit. Section II gives the open loop and closed loop simulation of the circuit with results. Section III gives the hardware implementation and results in open loop and closed loop. Section IV gives conclusion.

2. ANALYSIS AND DESIGN OF THE CONVERTER

Fig. 3 is the circuit configuration of proposed dual input modified SEPIC converter. The converter is analysed in three operating modes. The circuit is analysed in steady state and continuous current mode operation. The gating signals for S1 and S2 are as shown in Fig. 4. During K1T switch 1 is ON, during KeffT switch 1&2 are OFF and during K2T switch 2 is ON. The passive lossless snubber circuit formed by inductors Ls, capacitor Cs and Cb, and diodes D1,D2 and D3 are significant only during the switching instant that reduce the transient dv/dt and di/dt across the device, the energy stored in the switching process is recovered.

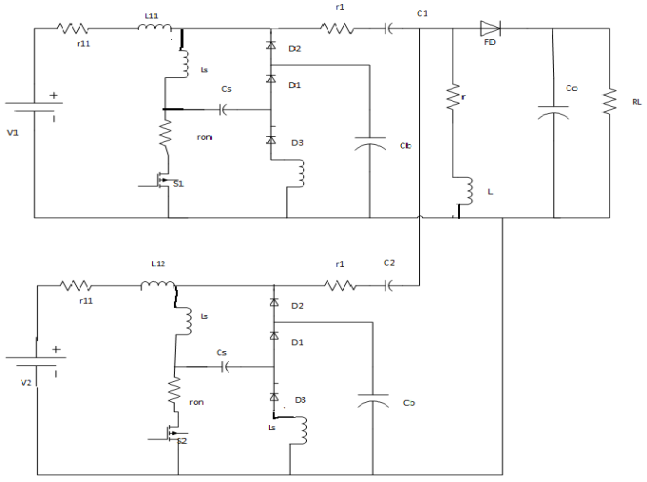


Fig 3: Circuit schematic of the topology

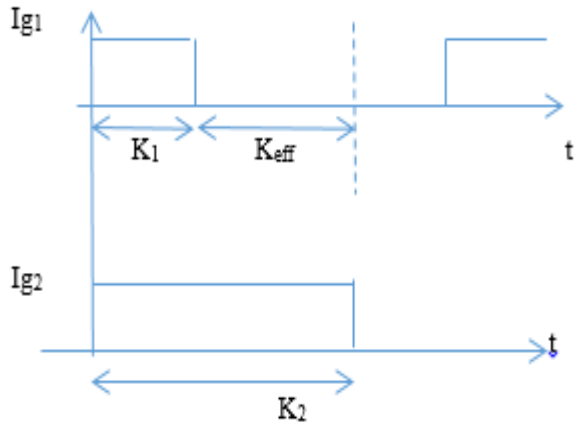


Fig 4: Gating pulses given to S_1 and S_2

A. State 1 ($0 < t < K_1T$)

Equivalent circuit of converter in this state is as shown in Fig. 5 (a). The two switches are given the gating but only S1 will conduct as the voltage across C1 reverse bias S2.The inductor current in L11 and L12 rises linearly. Output capacitor supplies load as output diode is off.

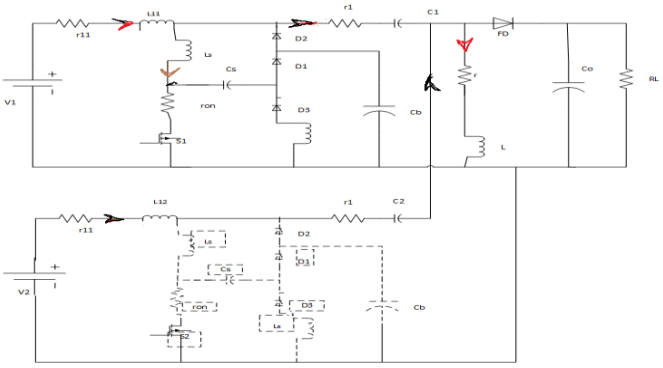


Fig 5 (a): Equivalent diagram in mode 1

The ripple current expression for the input inductor L_{11} and L_{12} is given by

$$\Delta IL_{11} = \left(\frac{V1 - VrL11}{L11}\right) K_1T \quad (1)$$

$$\Delta IL_{12} = \left[\frac{(V2 + Vc1 - Vc2) - VrL12 - VrC2 - Vrc1}{L12}\right] K_1T \quad (2)$$

B. State 2 ($K_1T < t < K_2T$)

Equivalent circuit of converter in this state is as shown in Fig. 5 (b). In this mode S_2 is on and S_1 is off. Current through L_{11} and L_{21} are increasing and free-wheeling diode D is still reverse biased thereby not conducting any current through it.

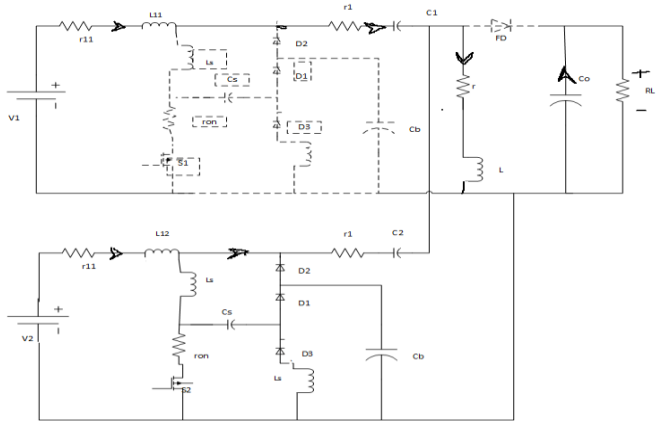


Fig 5(b): Equivalent diagram in mode 2

The ripple current equations are given by

$$\Delta IL_{11} = \frac{(V1 - Vc1 + Vc2) - Vr1 - Vrc1 - Vrc2}{L12} (K_2 - K_1)\, T \quad (3)$$

$$\Delta IL_{12} = \frac{V2 - VrL12}{L12} K_{2eff} T \quad (4)$$

C. State 3 ($D_2T < t < T$)

Equivalent circuit of converter in this state is as shown in Fig. 5(c). In this mode both the devices are off. Free-wheeling diode D is forward biased, the energy stored in inductors is delivered to load.

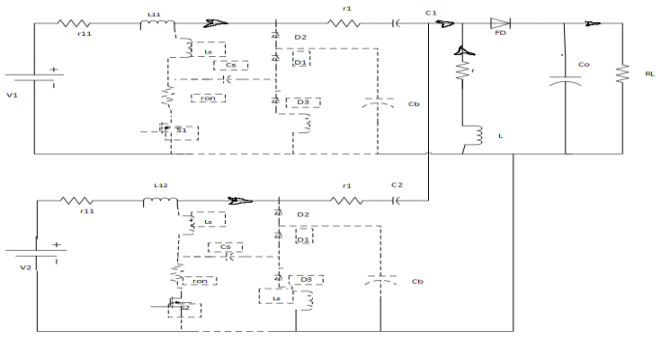


Fig 5(c) : Equivalent circuit in mode 3

The ripple current equations are

$$\Delta IL_{11} = \frac{(V1-VrL11-Vrc1-Vo)}{L11}(1-K_2)\,T \qquad (5)$$

$$\Delta IL_{12} = \frac{V2-VrL12-Vrc2-Vo}{L12}(1-K_2)\,T \qquad (6)$$

From these equations the average output voltage is obtained as

$$Vo = \frac{(V1-VrL11-VrL12)(K1)+V2(K2-K1)-VrC1(1-K1)-VrC2(K2-K1)}{Vo(1-K2)} \qquad (7)$$

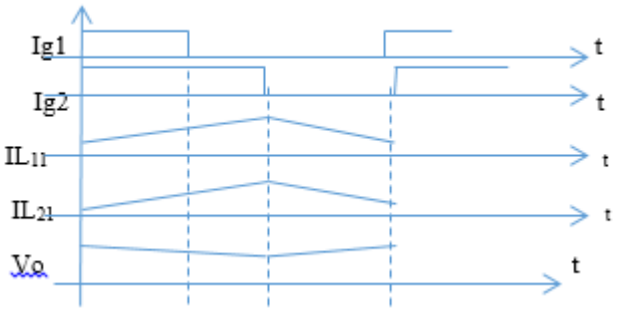


Fig 6: Waveforms of current through inductor L_{11}, L_{21}, output voltage, duty cycle of switches

Design

The design of the converter components requires mainly the specifications. Table 2 gives the parameter specification used for the design.

Table 2: Specifications of the converter

Sl. No.	Pecifications	Value
1	Input voltage 1	20-30V,50W
2	Input voltage 2	10-20V,50W
5	Switching frequency	150 k Hz
6	Output voltage	12V
7	Ripple voltage	5%
8	Ripple current	10%
7	Load	100 watts
8	Efficiency	≥90%

K_1 is calculated by keeping V_2=0 V in equation (7) and similarly K_2 is calculated by keeping V_1=0 V

K_1 = 66.7%, K_2 = 78%

The input inductance is given by

$$L_{11} = \frac{V_1 D_1}{\Delta I_{L1} f} \qquad (8)$$

Substituting respective values in above equation,

L_{11}=19.24 mH

Similarly, L_{21} = 6 mH

The input capacitance is given by

$$C_1 = \frac{V_o D_1}{R \Delta V_0 f} \qquad (9)$$

Substituting respective values in above equation,

C_{11} = 361.32 µF

Similarly, C_{21} = 434 µF

3. SIMULATION & RESULTS

The proposed converter is simulated in MATLAB in open loop under variable source conditions keeping load constant and variable load conditions keeping source constant with adjustable duty ratio to maintain output voltage constant. The simulation circuit is as shown in Fig 6. For each case the parameters like voltage ripple, current ripple, efficiency and voltage stress across the device are tabulated. The parameter list are as shown in the Table 3, Table 4 and table 5.

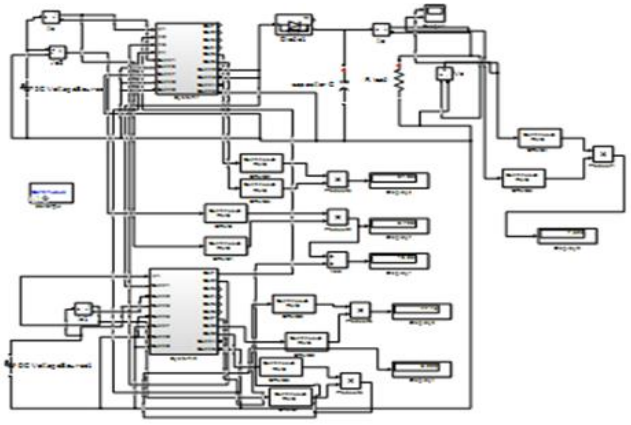


Fig 6: Simulink circuit of proposed topology

Table 3: List of parameters for Variation of input source 1 and keeping V_2 fixed

V_1	V_2	K_1	K_2	Vo	Io	ΔVo	ΔIo	η	Stress across S1	Stress across S2
20	20	37	50	12.4	6.2	0.3	0.145	87.2	107.2	168
21	20	35	50	12.35	6.3	0.29	0.07	87.12	109	163
22	20	33	50	12.3	6.14	0.29	0.15	87.01	106	163
23	20	31	51	12.42	6.2	0.3	0,15	86.96	108	165
24	20	30	52	12.6	6.29	0.33	0.15	86.6	107	166
25	20	29	53	12.8	6.38	0.3	0.15	86.37	105	169
26	20	28	54	12.35	6.2	0.3	0,15	80.83	108	165
27	20	27	54.5	12.9	6.4	0.31	0.14	86.1	107	166
28	20	26	53	12.65	6.34	0.29	0.15	85.8	105	169
29	20	25	53.5	12.45	6.24	0.32	0.16	86.8	109	163
30	20	20	56	12.75	6.38	0.29	0.14	83.7	106	163

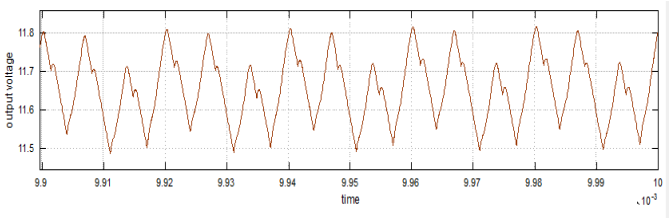
Table 4: List of parameters for Variation of input source 2 and keeping V_1 fixed

V_1	V_2	K_1	K_2	Vo	Io	ΔVo	ΔIo	η	Stress across S1	Stress across S2
30	15	25	66	11.2	5.48	0.26	0.14	76.9	278	227
30	16	24.5	65	11.5	5.74	0.27	0.14	77.25	275	256
30	17	24.5	64	12.1	6.06	0.302	0.16	78.7	272	248
30	18	24	63	12.7	6.35	0.25	0.15	80.2	270	250
30	19	25	59	12.9	6.48	0.3	0.15	83.6	267	240
30	21	26	51	12.8	6.44	0.3	0.15	85.8	271	245

Table 5: List of parameters keeping sources constant and varying Load resistance

V_1	V_2	K_1	K_2	V_o	Io	Load R	ΔVo	ΔIo	η	Stress across S1	Stress across S2
30	20	20	56	12.75	6.38	2	0.15	0.18	82	165	95
30	20	30	47	12.68	3.165	4	0.16	0.18	81.3	167	94
30	20	29	46	12.54	2.51	5	0.12	0.023	77.8	129	92.3
30	20	28	45	12.28	2.045	6	0.1	0.012	73.2	148	82.3
30	20	27	44	11.94	1.704	7	0.14	0.13	75.6	139	68

In the proposed converter, feedback PID controller is used for controlling the constant output voltage in variations of input voltage sources and load. It also transfers energy to the load individually or simultaneously. In order to improve the efficiency and reducing the ripple content of output voltage and current, Ziegler and Nichols tuning method of PID controller is tuned properly to maintain output voltage constant with variations of input voltage and load. The PID parameters are designed by Ziegler – Nichols tuning method to regulate the output voltage. There are two way of finding controller parameters using Ziegler and Nichols tuning method. That is one way of finding parameters by transfer-function method and other by trial and error tuning method. In this project, controller parameters are tuned by trial and error method based on sustained oscillations.



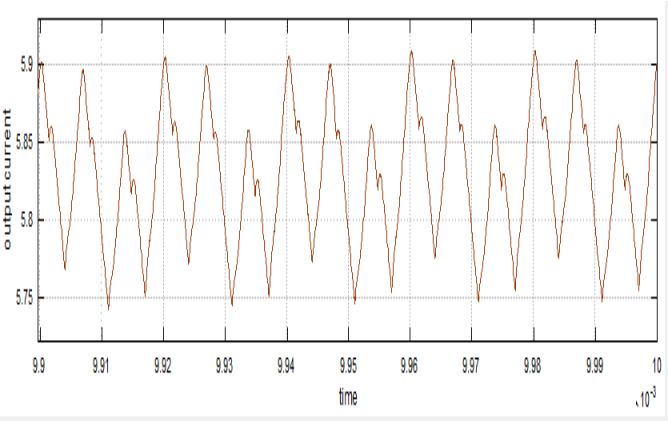


Fig 7: waveforms of output voltage and output current

Table 6: List of parameters in closed loop keeping V_2 constant and V_1 varying

V_1	V_2	P_1+P_2	Po	Vo	Io	ΔVo	ΔIo	η	Stress across S_1	Stress across S_2
20	20	6.1+61.9=68	55.5	10.9	5.1	0.29	0.17	81.6	110	220
22	20	8.12+61.6=69.7	57.3	11.1	5.2	0.22	0.16	82.2	124	226
23	20	9.5+61.3=70.8	58.2	11,2	5.3	0.23	0.15	82.2	138	228
24	20	10.6+61.3=71.9	58.9	11.29	5.2	0.33	0.15	81.9	137	230
25	20	12.1+61.08=73.2	59.8	11.4	5.4	0.3	0.13	81.8	139	233
26	20	13.5+60.4=73.9	60.74	11.7	5.6	0.28	0.15	82.2	159	235
27	20	15.9+58.4=74.3	61.58	11.8	5.7	0.31	0.14	82.8	170	234
28	20	19+57=76	62.6	11.7	5.4	0.29	0.15	82.3	178.8	236
29	20	20.1+56=76.1	63	11.75	5.84	0.33	0.16	82.7	188	235
30	20	24.6+52=76.6	63.6	11.65	5.87	0.3	0.15	83.1	198	232

Table 7: List of parameters in closed loop keeping V_1 constant and V_2 varying

V_1	V_2	P_1+P_2	Po	Vo	Io	ΔVo	ΔIo	η	Stress across S1	Stress across S2
30	20	24.6+52=76.6	63.6	11.65	5.87	0.3	0.15	83.1	198	232
30	21	21.9+62=83.9	70	12.2	6.2	0.32	0.14	83.4	203	260
30	22	20.1+70.26=90.4	74	12.5	6.3	0.29	0.16	81.8	209	284
30	19	25.14+46.38=71.5	60	11.35	5.8	0.3	0.17	83.9	192	212
30	18	25.5+40.53=66	54.6	10.8	5.4	0.32	0.16	82.7	187	194
30	17	24.6+34.6=59.2	50	10.5	5.2	0.32	0.15	84.5	185	195

Table 8: List of parameters in closed loop keeping V_1 & V_2 constant and varying Load

V_1	V_2	R_L	P_1+P2	Po	Vo	Io	ΔVo	ΔIo	η	Stress across S1	Stress across S2
30	20	2.5	20.68+53.3=73.9	63	12.6	5.14	0.33	0.14	85.5	198	232
30	20	2	24.6+52=76.6	63.6	11.65	5.87	0.3	0.15	83.1	198	232
30	20	4	17.5+47.3=64.8	58	15	3.4	0.29	0.16	89	143	183
30	20	3	18.6+52.3=70.9	60.1	13.7	4.6	0.3	0.17	84.5	159	193
30	20	5	14.2+30.8=45	37.5	13.6	4.3	0.32	0.16	83.3	187	194

4. HARDWARE IMPLEMENTATION & RESULTS

The proposed dual input modified SEPIC converter under closed loop is implemented with DSP processor as per the designed specifications. For generating switching pulses Cortex M4 processor is used. The feedback from the output load is fed to the cortex M4 processor. It is programmed to obtain the gating pulses for switches in order to maintain output voltage constant at 12V with variations of two input voltages that fed to the two switches through driver circuit.. The algorithm is initially set system control configuration that defines the pin number for pulses, Vcc, ground point and configuring CPU timer. Then setting the parameters Kp, Ki of PID controller and set required PWM for12V. Start with ADC bit and compare with set point. Now calculate control voltage PWM that gives the gate pulses. If the pulses are not satisfied with set point then gate pulse is feedback to the comparison of ADC.

The results of hardware implementation of proposed converter cortex M4 processor under closed loop are observed. The DSP processor is programmed in such a way that the output voltage is maintained constant at 12V in variation of input voltage V1 in the range of 20V-30V and V2 in the range of 15V-25V with proper tuning of PID parameters. Fig 7 shows the output voltage and Fig 8 shows the voltage waveform of the switches. The parameters are tabulated in Table 10.

Fig 8: Image of prototype of hardware implementation

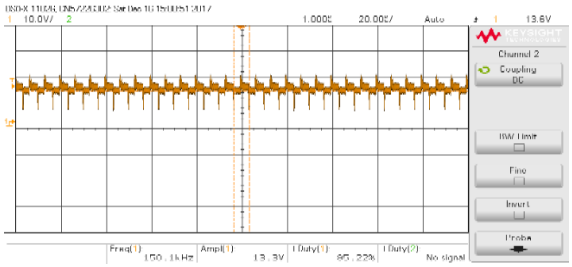


Fig 7: Output voltage waveform

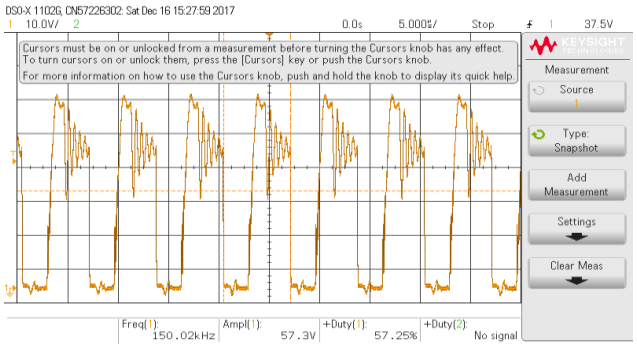


Fig 8: output voltage waveform

Table 10: listing of parameters

V_1	V_2	V_0	ΔV_0	I_O	P_O	P_S	EFFICIENCY
30	20	13.3	2V	2.4	31.92	38	84
32	23	11.9	2.3	2.5	29.75	36	82.6
35	25	11.7	2.4	2.4	28.08	36	78
25	--	13.2	1.8	2.4	31.68	37.5	85.5
--	20	13	3.2	2.2	36	40	90

5. CONCLUSION

Power Electronics basically controls and converts electrical power from one form to the other. They are widely used in applications like power generation, transmission and distribution systems.. The multiple input converters (MICs) are utilized in place of various individual single input converters due to less complex circuit, cost and maintenance. The dual input SEPIC-SEPIC converter is selected based on the better efficiency and low current ripple as compared with other converter topologies. The proposed dual input SEPIC converter is analysed in both open and closed loop scenario. In open loop, the output voltage is maintained constant by varying gating signals of two switches with variations of two input sources. In closed loop, the output voltage is maintained constant by feedback controller with variations of two input sources. The feedback controller is controlled by one of the method of PID tuning technique. The PID parameters are obtained by trial and error method of Zeigler and Nichols tuning method. The hardware circuit is implemented using Cortex M4 processor that operates as a controller. The experimental result measured in hardware implementation is approximately closed to the simulated values in both open and closed loop. By changing the input voltages, the output voltage is maintained constant at 12V with ripple of 0.02V and output current is measured at 4A. The efficiency of proposed converter is 85%.

REFERENCES

[1] Nithya. K and M. Ramasamy, "Modeling of Multi-Input DC-DC Converter for Renewable Energy Sources" International Journal of Innovative Research in Science, Engineering and Technology, Rasipuram, Tamilnadu, India, vol. 3, no. 1, Feb 2014.

[2] Hamid Behjati and Ali Davoudi "Discrete-time Modeling of Multiple-input DC Energy Conversion Systems", IEEE Electric Ship Technologies Symposium (ESTS), Arlington, pp. 66-70, 2013.

[3] Lalit Kumar, Shailendra Jain and M.A.N.I.T.Bhopal, "A Novel Dual Input DC-DC Converter Topology", IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES), Bengaluru, India, pp. 1-6, 2012.

[4] Chimaobi N. Onwuchekwa, and Alexis Kwasinski "A Modified-Time-Sharing Switching Technique for Multiple-Input DC–DC Converters" IEEE transactions on Power Electronics, vol. 27, no. 11, pp. 4492 – 4502, Nov 2012.

[5] Yaow-Ming Chen, Yuan-Chuan Liu, and Feng-Yu Wu," Multi-Input DC/DC Converter Based on the Multiwinding Transformer for Renewable Energy Applications", IEEE Transactions On Industry Applications, Vol. 38, No. 4, July/August 2002

[6] Yuan-Chuan Liu and Yaow-Ming Chen, "A Systematic Approach to Synthesizing Multi-Input DC–DC Converters" IEEE transactions on Power Electronics, vol.24, no. 1, pp. 116 - 127, Jan 2009.

[7] Yan Li, Xinbo Ruan, Dongsheng Yang, Fuxin Liu and Chi K. Tse, "Synthesis of Multiple-Input DC/DC Converters" IEEE transactions on Power Electronics, vol. 25, no. 9, pp. 2372-2385, Sept 2010.

[8] Seung H. Choung, , IEEE and Alexis Kwasinski, "Multiple-Input DC-DC Converter Topologies Comparison", Industrial Electronics, 2008. IECON 2008. 34th Annual Conference of IEEE, Orlando, FL, USA, DOI: 10.1109/IECON.2008.4758325.

[9] Yaow-Ming Chen, Yuan-Chuan Liu, Shih-Chieh Hung, and Chung-Sheng Cheng, "Multi-Input Inverter for Grid-Connected Hybrid PV/Wind Power System", IEEE Transactions On Power Electronics, Vol 22, No 3, May 2007.

[10] Joanne Hui*, IEEE Student Member, Alireza Bakhshai, IEEE Senior Member, and Praveen K. Jain, IEEE Fellow," A Hybrid Wind-Solar Energy System: A New Rectifier Stage Topology, Applied Power Electronics Conference and Exposition (APEC), 2010 Twenty-Fifth Annual IEEE, Palm Springs, CA, USA,DOI: 10.1109/APEC.2010.5433678

[11] K. Mark Smith Jr. and K. M. Smedley, "Properties and Synthesis of Passive, Lossless Soft-Switching PWM Converters", 1st International Congress in Israel on Energy Power & Motion Control, 1997.

[12] Hemalatha J N, Hariprasad S A and G S Anitha "Analysis and Evaluation of Performance Parameters of Modified Single Ended Primary Inductance Converter", International Journal of Power Electronics and Drive Systems, vol 8, pp1585, December 2017.

Authors

Hemalatha J N, received B.E degree in Electrical Engineering in 1997and M.E (Power Electronics) in 2001 from Bangalore University. Her research interests are Power Electronic applications in Renewable energy resources and Education.

Dr. Hariprasad S A Obtained B.E degree in the year 1991 and M.E in the year 2000, completed Ph.D. degree in the year 2011 and two additional highest degrees, Doctor of science degrees in the year 2013 and 2014 for the post-doctoral research work on communication and embedded systems. Published 60 papers in International and National Journals / conferences and a text book on Advanced microprocessor. Established industry supported labs. Served as visiting professor to various reputed colleges in Bangalore.

Dr G S Anitha, received BE degree in Electrical Engineering, M.E from Bangalore University and PhD in 2010 from Avinashilingam Deemed University. She is currently an Associate Professor in the Department of Electrical & Electronics Engineering at R V College of Engineering. Her research interest in in the area of power systems, renewable energy, high voltage, electrical machines. Etc.,